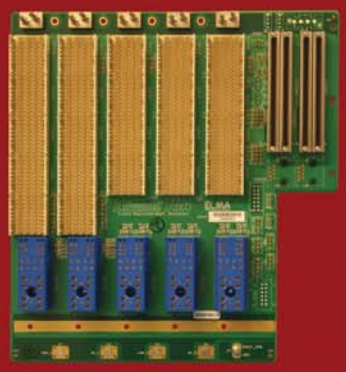
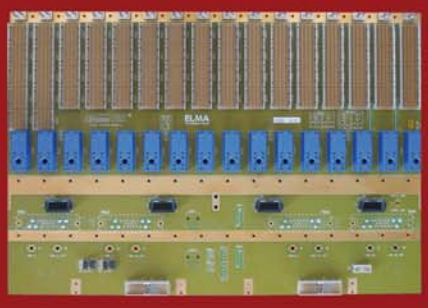
Elma Bustronic ATCA

User Manual





ATCA USER MANUAL

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Background

In the PICMG arena, CompactPCI has been a key backplane-based technology. It grew rapidly from its introduction in 1998 until the Telecom crash. With higher pin counts, Eurocard form factor, and hot swap capability, it has been a great open specification for Communications systems. With 33 Mhz processors limited to 8-slots over cPCI backplanes (without bridging) and 66 Mhz limited to 5-slots, the PICMG 2.0 specifications started to run into its performance limitations. The PICMG 2.16 and PICMG 2.17 specifications, running Ethernet and StarFabric fabrics respectively, have boosted the performance and reliability and will extend CompactPCI's life. But, PICMG realized its market needs even higher bandwidth and saw the Telecom Central Office as a key segment. Therefore, AdvancedTCA was introduced in the Fall of 2002. Switch cards from various vendors have been hitting the market since late 2003 and the technology appears to be taking off.

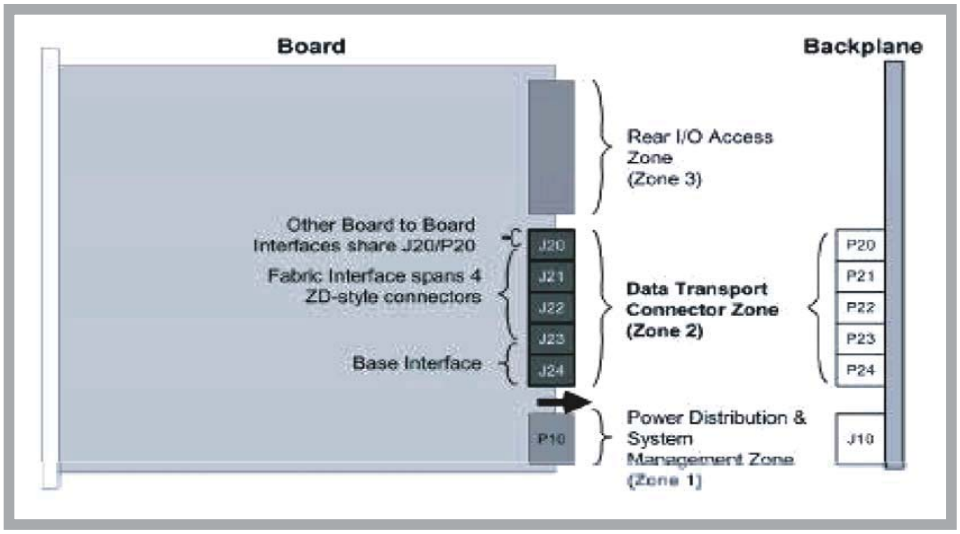
AdvancedTCA is the major initiative from PICMG, with over 125 members participating. The 8U x 280mm cards and 1.2" pitch allow large server blades with a wealth of components to be used. The technology utilizes primarily Dual Star (two hubs slots with direct links to each of the node slots) and Mesh switched fabric topologies (each slot acts as a hub slot, with direct links to every other slots, vastly increasing the bandwidth). The architecture will be able to handle interfaces up to 40Gpbs (for Terabit backplane bandwidth), High Availability (99.999% uptime), and Quality of Service issues demanded by the telecom central office. Geared towards CO applications, the backplane allows for 48VDC input from an external source to be distributed to the individual slot cards. The PICMG 3.0 core specification for AdvancedTCA has been ratified since late 2002. The sub-specifications for Ethernet (PICMG 3.1), Infiniband (PICMG 3.2), StarFabric (PICMG 3.3), and PCI Express (PICMG 3.4) have also been ratified. A new sub-specification for RapidIO over ATCA has been announced - PICMG 3.5. PICMG sponsors hope that base ATCA will become an all-encompassing architecture for network architectures from the Data Center to the Core to the Access Edge.

ATCA Performance

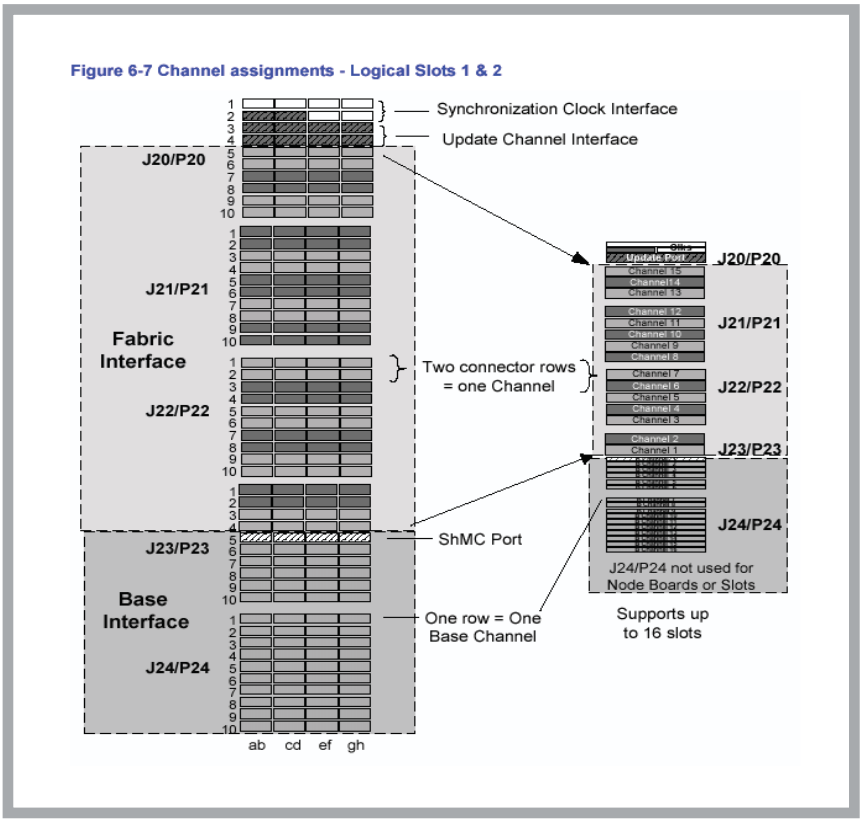
Among the main goals for ATCA were to offer a viable solution for a host of performance limiting drawbacks of other architectures. For example, the insufficient board space to package the requisite functionality, narrow board spacing (pitch), limited backplane throughput, demanding levels of signal integrity and EMC, inadequate system management modules (both h/w and s/w) and lack of scalability in capacity, reliability and performance. The advent of ATCA offers compelling reasons to select it as the platform of choice carrier-grade operating systems. ATCA boasts the following:

- High speeds scalable to 2.5Tb/sec.
- High Availability – RAS (Reliability, Availability and Serviceability) functionality by virtue of Redundancy, Failover, Fault prediction and prevention
- Open standards
- Interoperable third party products contributing to a dynamic ecosystem
- Robust system management features
- Scalable and cost effective

ATCA Form Factor and Zones



The ATCA backplane is broken up into zones. Zone 1 contains the power connector as well as the redundant IPMB's. Zone 2 is made up of the signal connectors carrying the base interface, clocks, update channel interface and the fabric interface. The base interface uses an Ethernet Dual Star topo ogy. Horizontally the connector columns have 5 differential pairs and vertically there are 10 rows. The ZD connector is specifically designed for high speed differential signaling, and is capable of speeds up to 5 Gbps. Zone 3 is for Rear Transition Modules.

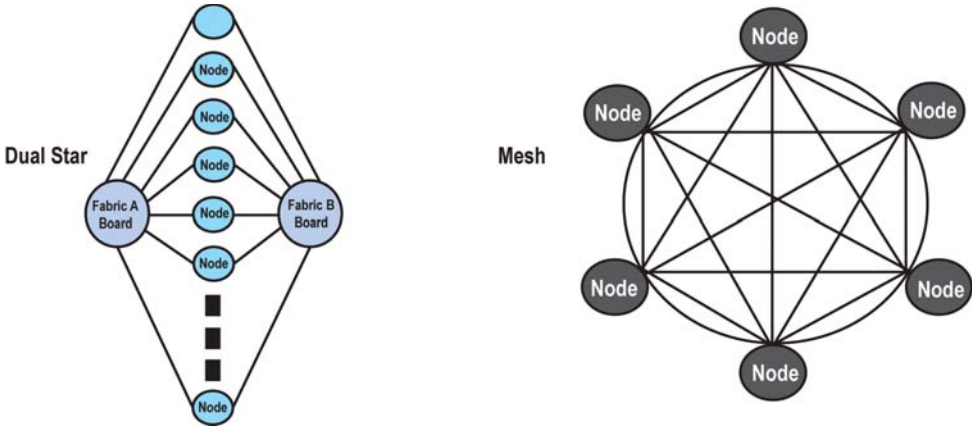


ATCA Topologies

AdvancedTCA specification allows a variety of architectural implementations. The topologies of the specification are Dual Star, Dual Dual Star, and Mesh (including Replicated Mesh). All of these configurations can go up to 14 slots (in a 19" rack). However, Replicated Mesh is limited to 8 slots. An ingenious channel mapping allows a standard ATCA switch card to support any configuration. For instance, a Dual Star (redundant hub slots running the fabric) implementation could be implemented with cards at either end of the subrack, adjacent in slots one and two or in the middle of the backplane.

The topology of the ATCA backplane can greatly affect the overall system cost as the cards, backplane, etc, will be affected. Focusing on the bac plane, a Mesh topology can demand significantly more layers than a Dual Star topology. With more point-to-point links, more layers need to be added to achieve the signal routing, which increase the cost of the backplane.

Dual Star, Dual-Dual Star, and Mesh configurations are available. See diagrams showing how nodes are interconnected in each topology.



Dual Star is a common topology with two fabrics slots, offering redundancy and helping achieve high availability. A Dual-Dual Star configuration has two sets of two fabric slots and offers multi-segment and multi-fabric options.

Dual Star topologies require two dedicated system slots (Fabric Slots) for the central switch Fabric Boards to reside. Each switch Fabric Board supports a Channel connection to all Node Boards in the system. Thus, each Node Board card has two Channels, one for each switch fabric. There is also a Channel connection between each Fabric Board. The number of Node Boards supported within a particular backplane implementation may vary up to a maximum of 14 total Node Boards/ Slots (in a 19" rack) which are connected to two dedicated switch Fabric Boards/Slots. In a PICMG 3.0 backplane the Base Interface is always routed as a Dual Star with Fabric Slots located in Logical Slots 1 & 2; the Fabric Interface minimum configuration is a Dual Star with Fabric Slots located in Logical Slots 1 & 2.

Dual Star Backplane Fabric Position

Dual Star Backplanes and Frames require installation of Fabric Boards to provide connectivity between Node Boards. PICMG 3.0 requires Fabric Boards to be installed into the lowest numbered Logical Slots (e.g. Slots 1 & 2). PICMG 3.0 systems may, however, have Fabric Slots/Boards located in any physical slot position. To facilitate system configuration, the Chassis FRU ROM is required to provide a mapping of Logical Slot positions to Physical slot positions.

Mesh

In a Mesh topology (where each node acts as a fabric slot, interconnected to the other with point-to-point links), the data rates and protocols are not dependent of other data transfers in other slots. So, it is highly scalable, forgoing latency and determinism problems. Mesh can be used in any slot size. However more slots used, the more difficulty in routing the numerous links. A 14-slot Mesh version would have very high layer counts and the expense of the backplane will rise. Therefore, Mesh configuration is, the attractive for smaller systems.

Mesh configurations do not utilize a central switch fabric; all system slots can be used for data forwarding or processing resources, which makes maximum use of the physical system capacity Another advantage of a full mesh is reduced start-up cost for partially equipped systems. Since the fabric capacity grows as you add system boards, there is no need to invest in expensive central fabrics that could have a great deal of unused capacity in lightly loaded systems, improving the economics of scaling. Further, all slots are identical, which eases installation and serviceability of the system. Mesh backplanes can support Star-based system configurations since Fabric Boards may be installed into logical slots 1 & 2. and Node Boards may be installed into all remaining slots just as done in a Dual Star Backplane.

Inspecting Your Backplane

Take great care when handling the backplane. Always use proper ESD handling procedures. Improper handling could cause damage to the connector pins. Always handle the backplane from the edges, never the connectors.

The first item that must be done before starting to utilize your backplane is to perform a thorough inspection. During the course of handling, shipping and assembly, pins, shrouds, mounting screws and other items could become damaged and/or loose. Operating a damaged backplane could cause serious damage to the backplane and/or devices that interface to it.

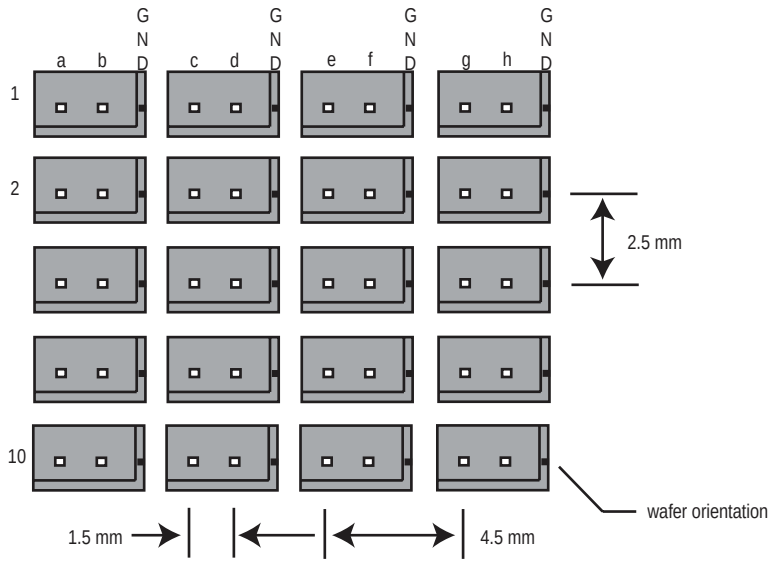
Take a few minutes to visually inspect that all of the connector pins are straight, screws are tight, etc. Repair any bent pins, shrouds, loose screws, etc. before proceeding. If the damage to the backplane is deemed too extensive, please call Elma Bustronic for assistance on how to proceed.

Installing Your Backplane In a Sub-Rack

Elma Bustronic ATCA backplanes use M3 Phillips head screws along the rows of mounting holes located at the top and bottom end of each slot. Install one screw in each hole and tighten securely. Do not install a screw in the mounting hole marked with a digital ground if a connection between chassis (safety) ground and digital (circuit) ground is not desired. The mounting hole that connects to digital ground is marked as *Shelf GND to Logical GND*. See Figure 1 below.

Zone 2 Connections

The Figure below illustrates the arrangement of signals on the ZD connector. The view is looking directly into the connector on the backplane.



2-Slot Mesh Pinouts

5U, 2-Slot, Mesh ATCA Backplane
Part# 109ATCA502

5VOUT	
1	5VOUT
2	SCL_A
3	SDA_A
4	GND
5	GND
6	SDA_B
7	SCL_B
8	5VOUT

SHMC	
1	E1RP
2	E1RN
3	E1TP
4	E2RP
5	E2RN
6	E1TN
7	E2TP
8	E2TN

I^2C/FTP/PEM	
1	I^2C_3_INT
2	I^2C_3_SCL
3	I^2C_3_SDA
4	FTP_0
5	FTP_2
6	PEM0
7	PEM1
8	FTP_3
9	FTP_1
10	I^2C_2_SDA
11	I^2C_2_SCL
12	I^2C_2_INT

Port E1 connects to 1SHMM1
Port E2 connects to 2SHMM1

FTFOUT/FILTER/PWM/TACH/SENSE	
1	FTFOUT_2
2	FTFOUT_0
3	FILTER0
4	PWM_0
5	PWM_2
6	TACH_0
7	TACH_2
8	TACH_4
9	TACH_6
10	NO CONNECT
11	-48VB3_SENSE
12	NO CONNECT
13	-48VA3_SENSE
14	NO CONNECT
15	-48VB4_SENSE
16	NO CONNECT
17	-48VA4_SENSE
18	-48VA4_RTN_SENSE
19	NO CONNECT
20	-48VB4_RTN_SENSE
21	NO CONNECT
22	-48VA3_RTN_SENSE
23	NO CONNECT
24	-48VB3_RTN_SENSE
25	NO CONNECT
26	TACH_7
27	TACH_5
28	TACH_3
29	TACH_1
30	PWM_3
31	PWM_1
32	FILTER1
33	FTFOUT_1
34	FTFOUT_3

RING

1	2	3	4
RRTN_B	-RING_B	RRTN_A	-RING_A

MT 2

4	3	2	1
MT2_RING	MT2_RING	MT2_TIP	MT2_TIP

MT 1

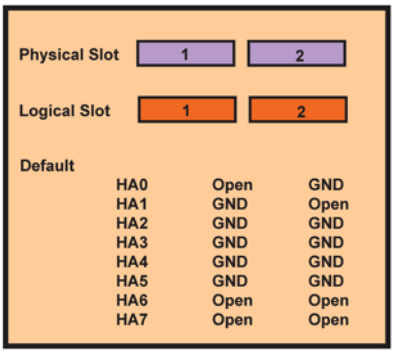
4	3	2	1
MT1_RING	MT1_RING	MT1_TIP	MT1_TIP

2-Slot Mesh Power Distribution

Physical Slot	1	2
Logical Slot	1	2
Source	A/B	A/B

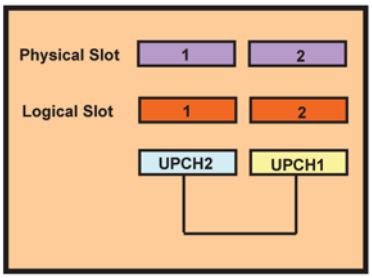
Hardware Address

5U, 2-Slot, Mesh ATCA Backplane
Part# 109ATCA502



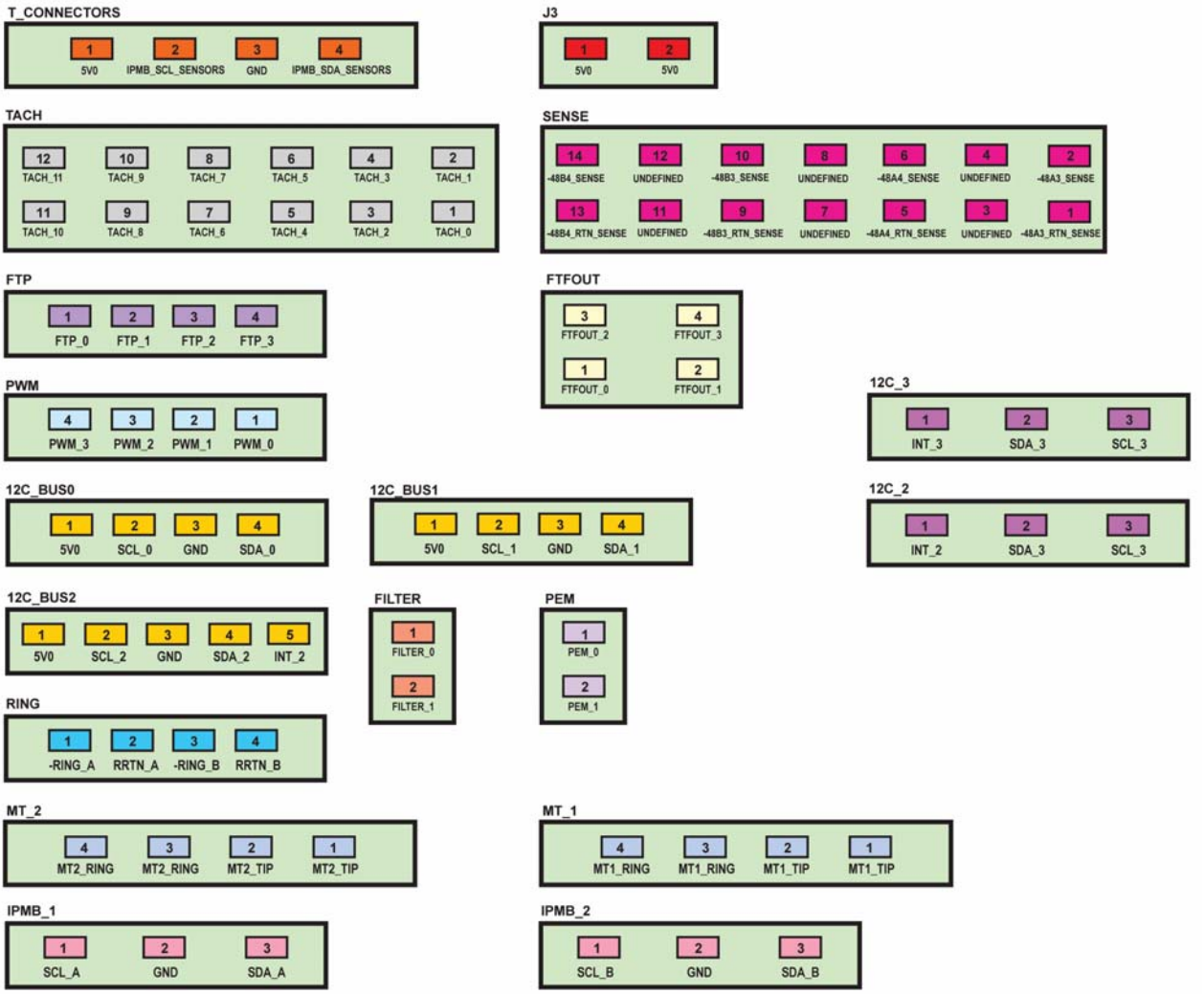
Update Channels

5U, 2-Slot, Mesh ATCA Backplane
Part# 109ATCA502



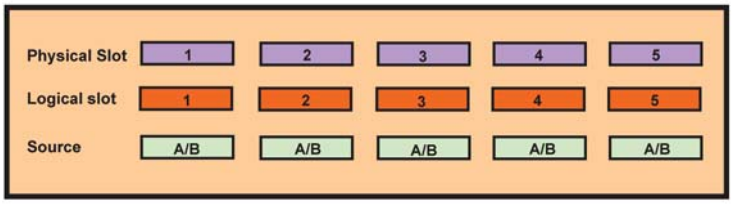
5-Slot Mesh Pinouts

5U, 5-Slot, Mesh ATCA Backplane
Part# 109ATCA505



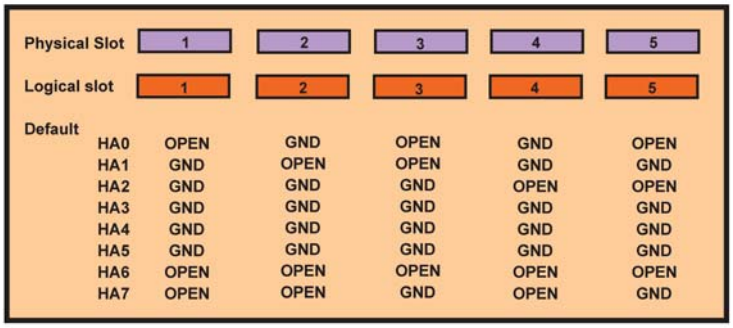
5-Slot Mesh Power Distribution

5U, 5-Slot, Mesh ATCA Backplane
Part# 109ATCA505



Hardware Address

5U, 5-Slot, Mesh ATCA Backplane
Part# 109ATCA505



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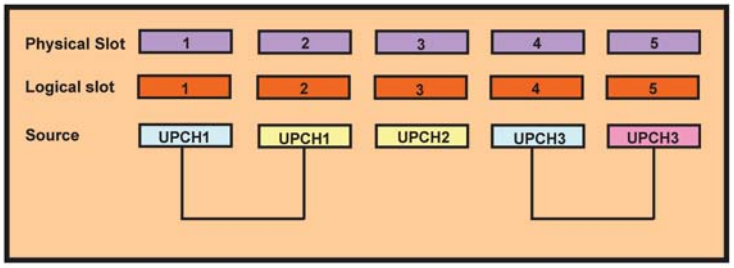
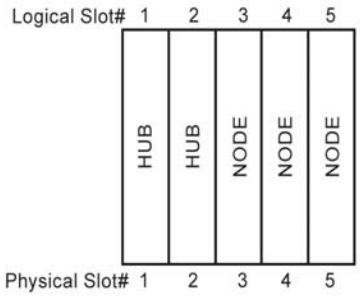
5U, 5-Slot, Mesh ATCA Backplane
Part# 109ATCA505



5-Slot Routing Table

Logical/Physical Slot#		1	2	3	4	5	
Connector	Channel						
P20	Fabric Ch 15	-	-	-	-	-	4th Fabric Mesh
P20	Fabric Ch 14	-	-	-	-	-	
P20	Fabric Ch 13	-	-	-	-	-	
P21	Fabric Ch 12	S5-CH9	S5-CH10	S5-CH11	S5-CH12	S4-CH12	3rd Fabric Mesh
P21	Fabric Ch 11	S4-CH9	S4-CH10	S4-CH11	S3-CH11	S3-CH12	
P21	Fabric Ch 10	S3-CH9	S3-CH10	S2-CH10	S2-CH11	S2-CH12	
P21	Fabric Ch 9	S2-CH9	S1-CH9	S1-CH10	S1-CH11	S1-CH12	
P21	Fabric Ch 8	S5-CH5	S5-CH6	S5-CH7	S5-CH8	S4-CH8	2nd Fabric Mesh
P22	Fabric Ch 7	S4-CH5	S4-CH6	S4-CH7	S3-CH8	S3-CH8	
P22	Fabric Ch 6	S3-CH5	S3-CH6	S2-CH6	S2-CH7	S2-CH8	
P22	Fabric Ch 5	S2-CH5	S1-CH5	S1-CH6	S1-CH7	S1-CH8	
P22	Fabric Ch 4	S5-CH1	S5-CH2	S5-CH3	S5-CH4	S4-CH4	Primary Fabric Mesh
P22	Fabric Ch 3	S4-CH1	S4-CH2	S4-CH3	S3-CH3	S3-CH4	
P23	Fabric Ch 2	S3-CH1	S3-CH2	S2-CH2	S2-CH3	S2-CH4	
P23	Fabric Ch 1	S2-CH1	S1-CH1	S1-CH2	S1-CH3	S1-CH4	
P23	Base Ch 1	ShMC	ShMC	S1-CH3	S1-CH4	S1-CH5	
P23	Base Ch 2	S2-CH2	S1-CH2	S2-CH3	S2-CH4	S2-CH5	
P23	Base Ch 3	S3-CH1	S3-CH2	-	-	-	
P23	Base Ch 4	S4-CH1	S4-CH2	-	-	-	
P23	Base Ch 5	S5-CH1	S5-CH2	-	-	-	

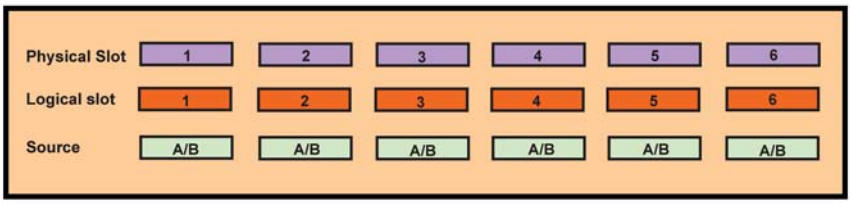
Legend: S = Slot #
Ch = Channel #



5-Slot Replicated Mesh Backplane Configuration

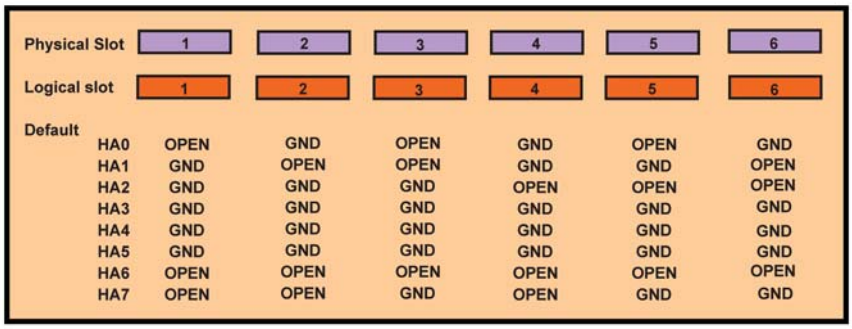
6-Slot Mesh Power Distribution

5U, 6-Slot, Mesh ATCA Backplane
Part# 109ATCA506



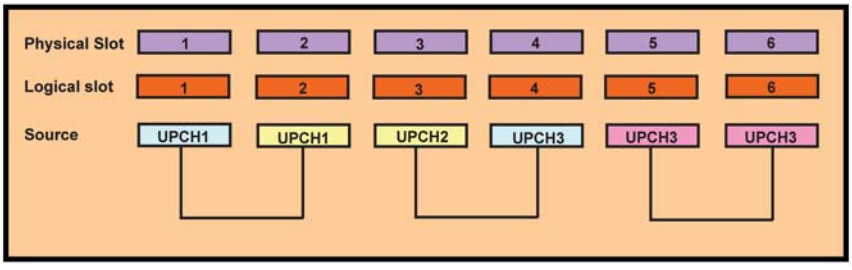
Hardware Address

5U, 6-Slot, Mesh ATCA Backplane
Part# 109ATCA506



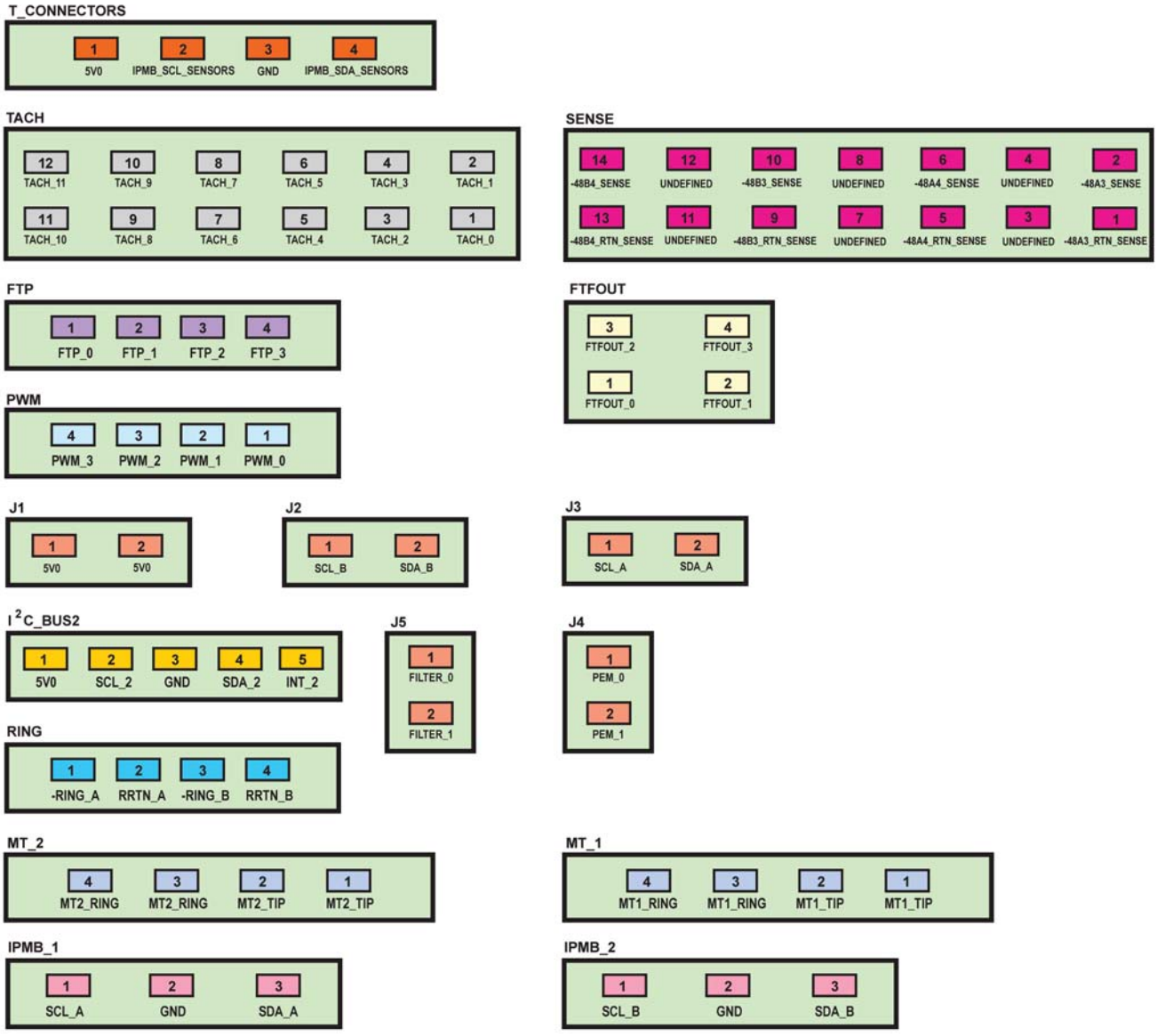
Update Channels

5U, 6-Slot, Mesh ATCA Backplane
Part# 109ATCA506



6-Slot Mesh Pinouts

5U, 6-Slot, Mesh ATCA Backplane
Part# 109ATCA506



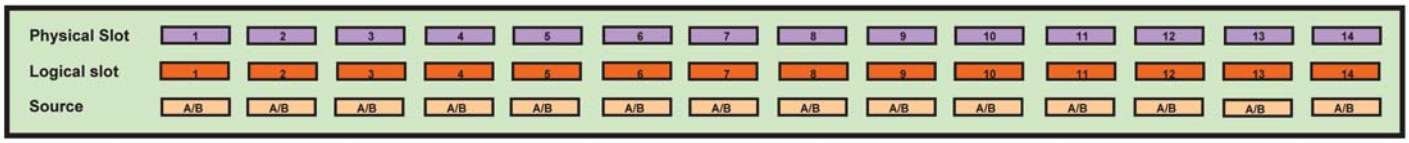
6-Slot Channel Mapping

Logical/Physical Slot#		1	2	3	4	5	6	
Connector	Channel							
P20	Fabric Ch 15	6-11	6-12	6-13	6-14	6-15	5-15	4th Fabric Mesh
P20	Fabric Ch 14	5-11	5-12	5-13	5-14	4-14	4-15	
P20	Fabric Ch 13	4-11	4-12	4-13	3-13	3-14	3-15	
P21	Fabric Ch 12	3-11	3-12	2-12	2-13	2-14	2-15	3rd Fabric Mesh
P21	Fabric Ch 11	2-11	1-11	1-12	1-13	1-14	1-15	
P21	Fabric Ch 10	6-6	6-7	6-8	6-9	6-10	5-10	
P21	Fabric Ch 9	5-6	5-7	5-8	5-9	4-9	4-10	
P21	Fabric Ch 8	4-6	4-7	4-8	3-8	3-9	3-10	2nd Fabric Mesh
P22	Fabric Ch 7	3-6	3-7	2-7	2-8	2-9	2-10	
P22	Fabric Ch 6	2-6	1-6	1-7	1-8	1-9	1-10	
P22	Fabric Ch 5	6-1	6-2	6-3	6-4	6-5	5-5	
P22	Fabric Ch 4	5-1	5-2	5-3	5-4	4-4	4-5	Primary Fabric Mesh
P22	Fabric Ch 3	4-1	4-2	4-3	3-3	3-4	3-5	
P23	Fabric Ch 2	3-1	3-2	2-2	2-3	2-4	2-5	
P23	Fabric Ch 1	2-1	2-1	1-2	1-3	1-4	1-5	
P23	Base Ch 1	ShMC	ShMC	1-3	1-4	1-5	1-6	
P23	Base Ch 2	2-2	1-2	2-3	2-4	2-5	2-6	
P23	Base Ch 3	3-1	3-2	-	-	-	-	
P23	Base Ch 4	4-1	4-2	-	-	-	-	
P23	Base Ch 5	5-1	5-2	-	-	-	-	
P23	Base Ch 6	6-1	6-2	-	-	-	-	

Format: Slot - Channel

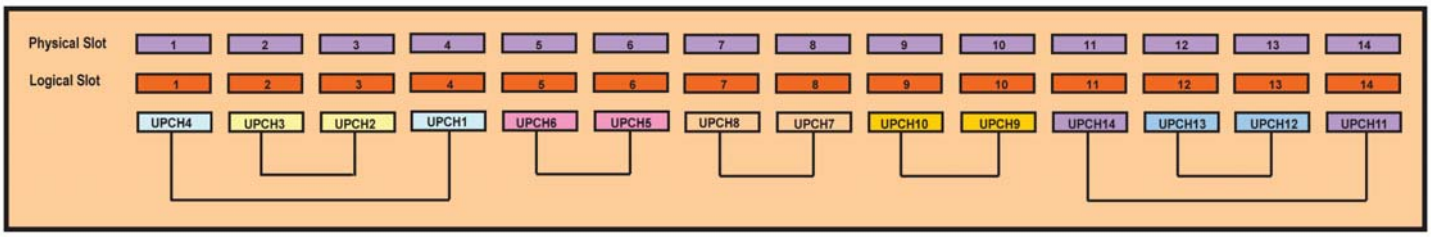
14-Slot Mesh Power Distribution

5U, 14-Slot, Mesh ATCA Backplane
Part# 1900001778



14-Slot Mesh Update Channels

5U, 14-Slot, Mesh ATCA Backplane
Part# 1900001778



14-Slot Mesh Routing Table

	Logical Slot #	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Connector	Channel #														
P20	14														
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13
P20	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13
P21	8	9-1	9-2	9-3	9-4	9-5	9-6	9-7	9-8	8-8	8-9	8-10	8-11	8-12	8-13
P22	7	8-1	8-2	8-3	8-4	8-5	8-6	8-7	7-7	7-8	7-9	7-10	7-11	7-12	7-13
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13
P22	5	6-1	6-2	6-3	6-4	6-5	5-5	5-6	5-7	5-8	5-9	5-10	5-11	5-12	5-13
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13

Note: The shading used in the above table shows discontinuity of the routing sequence across rows and columns in the table.

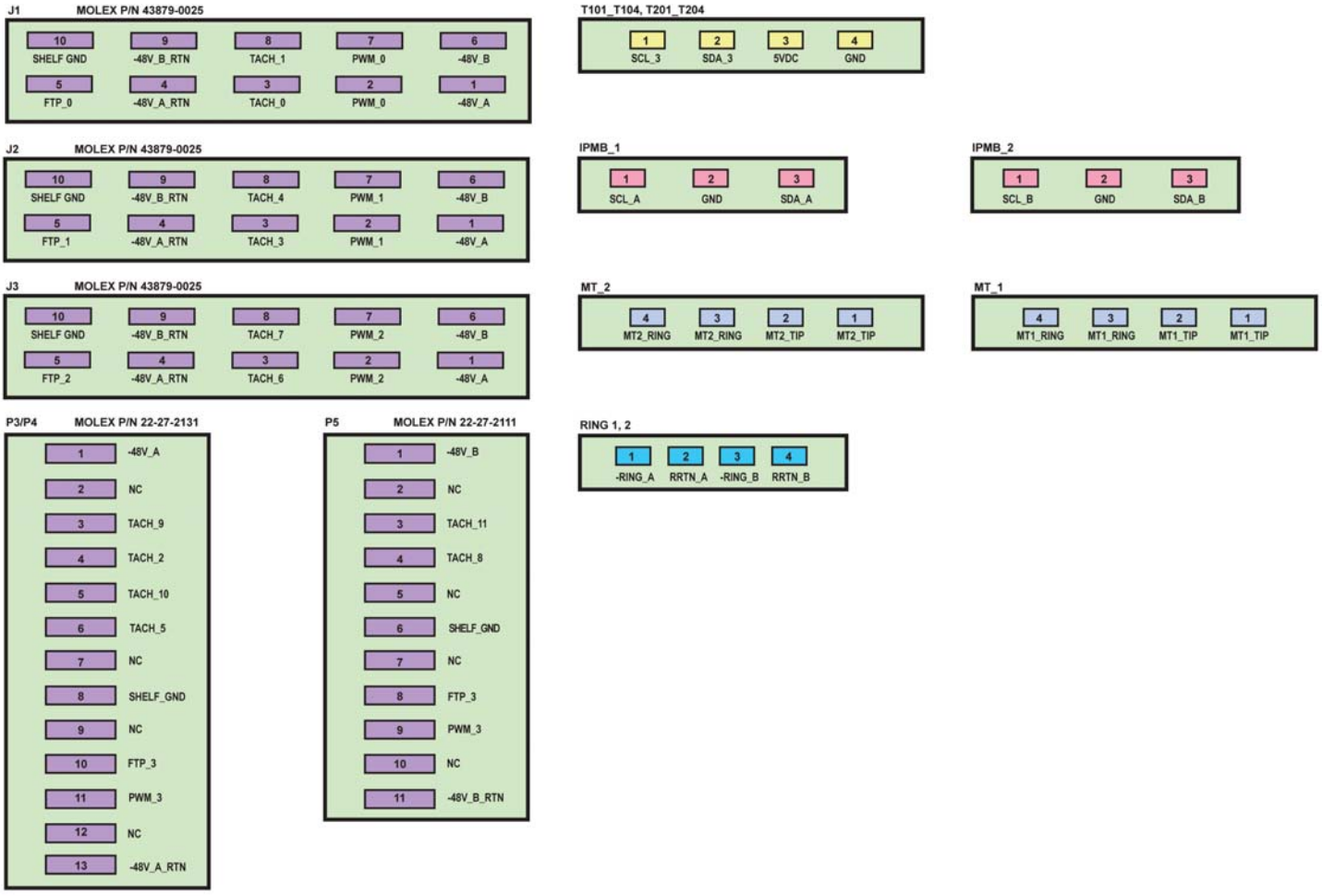
A Dual Star or Dual-Dual Star backplane will use a sub-set of this same Channel routing method. In the case of the Dual Star backplane, only those between slots 1 & 2 are required. The Full Mesh backplane is capable of supporting Mesh and Star system topologies determined by the types of boards installed. For example, a Dual Star system configuration is created by installing Hub Boards into Logical Slots 1 & 2 and Node Boards into all other slots.

Fabric Interface Dual Star

A backlane that supports only Dual Star configuration results from a Full Mesh backplane by depopulating all routing traces and backplane connectors except those that connect Channels 1 & 2 of each node slot to the Logical Slots 1 & 2 (Hub Slots) and those that connect Logical Slot 1 to Logical Slot 2. In a Dual Star backplane, Logical Slots 1 & 2 are dedicated as Hub Slots with up to 15 Channels each and all other Slots (up to 14) are Node Slots with Channels 1 & 2 mapped to the Hub slots.

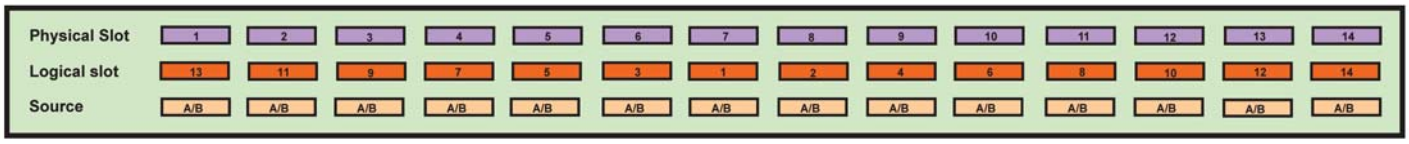
14-Slot Dual Star Pinouts

5U, 14-Slot, Dual Star ATCA Backplane
Part# 109ATCA514



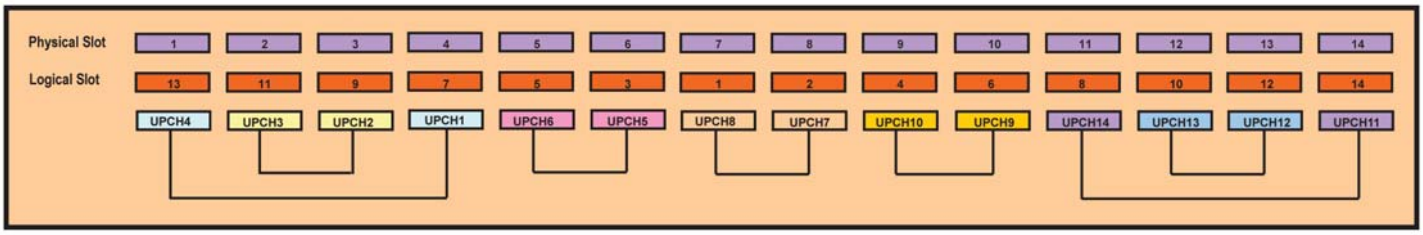
14-Slot Dual Star Power Distribution

5U, 14-Slot, Dual Star ATCA Backplane
Part# 109ATCA514



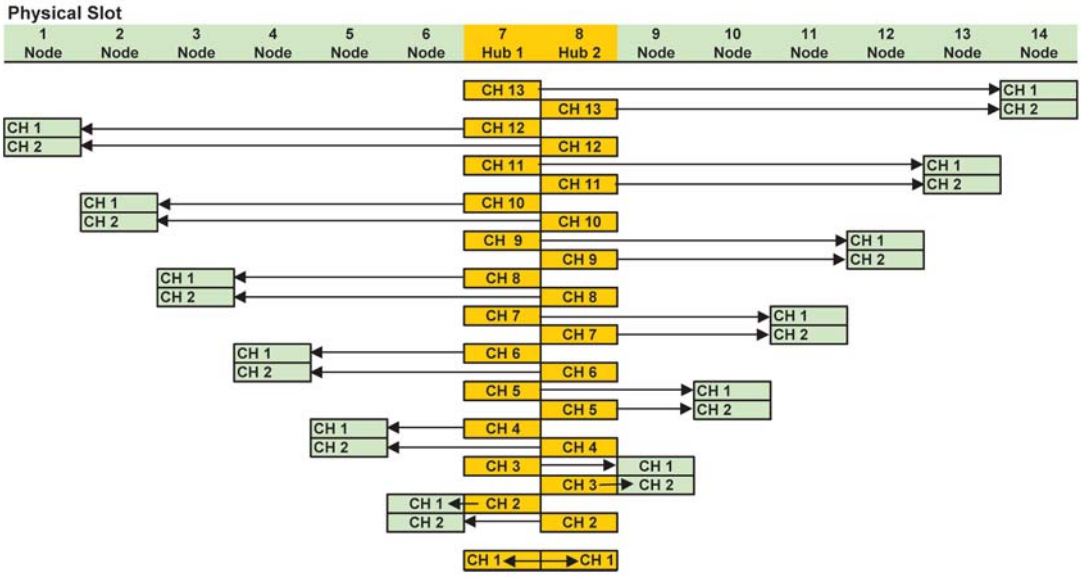
14-Slot Dual Star Update Channels

5U, 14-Slot, Dual Star ATCA Backplane
Part# 109ATCA514



14-Slot Dual Star Routing Diagram

5U, 14-Slot, Dual Star ATCA Backplane
Part# 109ATCA514



SHMC to Base Channel Jumper Configuration

7U, 14-Slot, Dual Star ATCA Backplane
Part# 109ATCA514

Configuration	Settings
Cross connect B open Ethernet port 1 of J4 SHMC 1 and J5 SHMC 2 connected	JP1-JP16 open R13-R20 installed R21-R28 not installed
Hub slot 7 (logical slot 1) SHMC cross connect B connected to J4 SHMC 1 Hub slot 8 (logical slot 2) SHMC cross connect B connected to J5 SHMC 2	JP1, JP3, JP5, JP7, JP10, JP12, JP14, JP16 installed JP2, JP4, JP6, JP8, JP9, JP11, JP13, JP15 open R13-R28 not installed
Hub slot 7(logical slot 1) SHMC cross connect B connected to J5 SHMC 2 Hub slot 8(logical slot 2) SHMC cross connect B connected to J4 SHMC 1	JP1 pin 1 to JP2 pin 1, JP1 pin 2 to JP2 pin 2 JP3 pin 1 to JP4 pin 1, JP3 pin 2 to JP4 pin 2 JP5 pin 1 to JP6 pin 1, JP5 pin 2 to JP6 pin 2 JP7 pin 1 to JP8 pin 1, JP7 pin 2 to JP8 pin 2 JP9 pin 1 to JP10 pin 1, JP9 pin 2 to JP10 pin 2 JP11 pin 1 to JP12 pin 1, JP11 pin 2 to JP12 pin 2 JP13 pin 1 to JP14 pin 1, JP13 pin 2 to JP14 pin 2 JP15 pin 1 to JP16 pin 1, JP15 pin 2 to JP16 pin 2 R13-R28 not installed

Shelf Manager Connector Pinout

5U, 2-Slot, Mesh ATCA Backplane, Part # 109ATCA502
5U, 5-Slot, Mesh ATCA Backplane, Part # 109ATCA505
5U, 6-Slot, Mesh ATCA Backplane, Part # 109ATCA506
5U, 14-Slot, Mesh ATCA Backplane, Part# 1900001778

Pin No.	Signal	Mating	Pin Function	Pin No.	Signal	Mating	Pin Function
85	NC	CutOut	No Connect	86	NC	CutOut	No Connect
84	NC	CutOut	No Connect	87	NC	CutOut	No Connect
83	-48V_A	FIRST	-48VDC A Input	88	-48VA_RTN	FIRST	-48VDC A Return
82	NC	CutOut	No Connect	89	NC	CutOut	No Connect
81	NC	CutOut	No Connect	90	NC	CutOut	No Connect
80	NC	CutOut	No Connect	91	NC	CutOut	No Connect
79	-48V_B	FIRST	-48VDC B Input	92	-48VB_RTN	FIRST	-48VDC B Return
78	NC	CutOut	No Connect	93	NC	CutOut	No Connect
77	-48V_A	FIRST	-48VDC A Input	94	-48VA_RTN	FIRST	-48VDC A Return
76	NC	CutOut	No Connect	95	NC	CutOut	No Connect
75	NC	CutOut	No Connect	96	NC	CutOut	No Connect
74	NC	CutOut	No Connect	97	NC	CutOut	No Connect
73	-48A3_SENSE	THIRD	-48V A3 Sense	98	-48A3_RTN_SENSE	THIRD	-48V A3 Sense Rtn
72	NC	CutOut	No Connect	99	NC	CutOut	No Connect
71	-48A4_SENSE	THIRD	-48V A4 Sense	100	-48A4_RTN_SENSE	THIRD	-48V A4 Sense Rtn
70	NC	CutOut	No Connect	101	NC	CutOut	No Connect
69	-48A5_SENSE	THIRD	-48V A5 Sense	102	-48A5_RTN_SENSE	THIRD	-48V A5 Sense Rtn
68	NC	CutOut	No Connect	103	NC	CutOut	No Connect
67	NC	CutOut	No Connect	104	NC	CutOut	No Connect
66	NC	CutOut	No Connect	105	NC	CutOut	No Connect
65	-48V_B	FIRST	-48VDC B Input	106	-48V_B_RTN	FIRST	-48VDC B Return
64	NC	CutOut	No Connect	107	NC	CutOut	No Connect
63	NC	CutOut	No Connect	108	NC	CutOut	No Connect
62	NC	CutOut	No Connect	109	NC	CutOut	No Connect
61	-48B3_SENSE	THIRD	-48V A3 Sense	110	-48B3_RTN_SENSE	THIRD	-48V B3 Sense Rtn
60	NC	CutOut	No Connect	111	NC	CutOut	No Connect
59	-48B4_SENSE	THIRD	-48V B4 Sense	112	-48B4_RTN_SENSE	THIRD	-48V B4 Sense Rtn
58	NC	CutOut	No Connect	113	NC	CutOut	No Connect
57	-48B5_SENSE	THIRD	-48V B5 Sense	114	-48B5_RTN_SENSE	THIRD	-48V B5 Sense Rtn
56	NC	CutOut	No Connect	115	NC	CutOut	No Connect
55	NC	CutOut	No Connect	116	NC	CutOut	No Connect
54	NC	CutOut	No Connect	117	NC	CutOut	No Connect
53	GND	FIRST	LOGIC GROUND	118	GND	FIRST	LOGIC GROUND
52	GND	FIRST	LOGIC GROUND	119	GND	FIRST	LOGIC GROUND
51	PWM0_OUT	THIRD	Fan PWM Signal	120	TACH5	SECOND	Fan Tachometer Signal
50	PWM1_OUT	THIRD	Fan PWM Signal	121	FTFOUT_6	SECOND	Fan tray fail signal
49	GND	FIRST	LOGIC GROUND	122	TACH6	SECOND	Fan Tachometer Signal
48	PWM2_OUT	THIRD	Fan PWM Signal	123	FTFOUT_7	SECOND	Fan tray fail signal
47	PWM3_OUT	THIRD	Fan PWM Signal	124	TACH7	SECOND	Fan Tachometer Signal
46	GND	FIRST	LOGIC GROUND	125	GND	FIRST	LOGIC GROUND
45	PRES#	LAST	Present Signal	126	TACH8	SECOND	Fan Tachometer Signal
44	FILTER0	SECOND	Air Filter Present Signal	127	TACH9	SECOND	Fan Tachometer Signal
43	FILTER1	SECOND	Air Filter Present Signal	128	TACH10	SECOND	Fan Tachometer Signal
42	R_PRES#	SECOND	Remote Present	129	TACH11	SECOND	Fan Tachometer Signal
41	FILTER2	SECOND	Air Filter Present Signal	130	GND	FIRST	LOGIC GROUND
40	FILTER3	SECOND	Air Filter Present Signal	131	PEM5	SECOND	PEM Present Signal
39	GND	FIRST	LOGIC GROUND	132	PEM4	SECOND	PEM Present Signal
38	L_HLY#	FIRST	Local Healthy	133	E1RN	THIRD	Ethernet 1 RX-
37	FTP_0	SECOND	Fan Tray Present Signal	134	E1RP	THIRD	Ethernet 1 RX+
36	FTP_1	SECOND	Fan Tray Present Signal	135	GND	FIRST	LOGIC GROUND
35	R_HLY#	FIRST	Remote Healthy	136	E1TN	THIRD	Ethernet 1 TX-
34	FTP_2	SECOND	Fan Tray Present Signal	137	E1TP	THIRD	Ethernet 1 TX+
33	FTP_3	SECOND	Fan Tray Present Signal	138	GND	FIRST	LOGIC GROUND
32	GND	FIRST	LOGIC GROUND	139	RX1N	THIRD	Ethernet 1 RX-
31	L_SWR#	FIRST	Local Switchover Request	140	RX1P	THIRD	Ethernet 1 RX+
30	FTP_4	SECOND	Fan Tray Present Signal	141	GND	FIRST	LOGIC GROUND
29	FTP_5	SECOND	Fan Tray Present Signal	142	TX1N	THIRD	Ethernet 1 TX-
28	R_SWR#	FIRST	Remote Switchover Request	143	TX1P	THIRD	Ethernet 1 TX+
27	PEM0	SECOND	PEM Present Signal	144	GND	FIRST	LOGIC GROUND
26	PEM1	SECOND	PEM Present Signal	145	SCL_A	THIRD	IPMB A
25	GND	FIRST	LOGIC GROUND	146	SDA_A	THIRD	IPMB A
24	HWA2	FIRST	Hardware Address	147	GND	FIRST	LOGIC GROUND
23	PEM2	SECOND	PEM Present Signal	148	SCL_B	THIRD	IPMB B
22	PEM3	SECOND	PEM Present Signal	149	SDA_B	THIRD	IPMB B
21	HWA1	FIRST	Hardware Address	150	GND	FIRST	LOGIC GROUND
20	L_PRES#	FIRST	Local Present	151	I2C_0_SCL	THIRD	Off board I2C bus
19	GND	FIRST	LOGIC GROUND	152	I2C_0_SDA	THIRD	Off board I2C bus
18	FTFOUT_0	SECOND	Fan tray fail signal	153	GND	FIRST	LOGIC GROUND
17	TACH0	SECOND	Fan Tachometer Signal	154	I2C_1_SCL	THIRD	Off board I2C bus
16	FTFOUT_1	SECOND	Fan tray fail signal	155	I2C_1_SDA	THIRD	Off board I2C bus
15	TACH1	SECOND	Fan Tachometer Signal	156	GND	FIRST	LOGIC GROUND
14	FTP_6	SECOND	Fan Tray Present Signal	157	I2C_2_SCL	THIRD	Off board I2C bus
13	FTP_7	SECOND	Fan Tray Present Signal	158	I2C_2_SDA	THIRD	Off board I2C bus
12	GND	FIRST	LOGIC GROUND	159	I2C_2_INT	THIRD	I2C Bus Interupt
11	5VOUT	LAST	5V Output	160	GND	FIRST	LOGIC GROUND
10	5VOUT	LAST	5V Output	161	I2C_3_INT	THIRD	I2C Bus Interupt
9	GND	FIRST	LOGIC GROUND	162	I2C_3_SCL	THIRD	Off board I2C bus
8	FTFOUT_2	SECOND	Fan tray fail signal	163	I2C_3_SDA	THIRD	Off board I2C bus
7	TACH2	SECOND	Fan Tachometer Signal	164	GND	FIRST	LOGIC GROUND
6	FTFOUT_3	SECOND	Fan tray fail signal	165	USB0P	THIRD	Primary USB+
5	TACH3	SECOND	Fan Tachometer Signal	166	USB0M	THIRD	Primary USB-
4	FTFOUT_4	SECOND	Fan tray fail signal	167	GND	FIRST	LOGIC GROUND
3	TACH4	SECOND	Fan Tachometer Signal	168	USBDP	THIRD	Secondary USB+
2	FTFOUT_5	SECOND	Fan tray fail signal	169	USBDM	THIRD	Secondary USB-
1	GND	FIRST	LOGIC GROUND	170	GND	FIRST	LOGIC GROUND

Signal Integrity Engineering

Faster PCB designs are by nature more sophisticated and delicate. At higher clock speeds, the PCB demands cleaner signal transmission without compromising the stability of the system. This is where Signal Integrity engineering comes into play. Simply put, signal integrity studies the design of high-speed circuits that can accommodate cleaner signals passing through them. Cleaner signals, in turn, enable engineers to identify and minimize sources of distortion in data transmission, which could otherwise disrupt timing of the digital logic. Signal integrity issues such as reflections, cross talk, frequency dependent transmission line loss and dispersion can significantly lead to poorer system performance propagating through the interconnect. These SI issues arise from via, power/ground coupling, RLC effects in signal lines, etc. With 3.125 Gbps to 6.250 Gbps signal speeds across the backplane and beyond, an AdvancedTCA backplane is very susceptible to these types of issues.

Below, we will show SI study examples on one of our AdvancedTCA backplanes, the 5-slot Mesh. These are just preliminary studies and the results or design may change at anytime. Consult the factory for further information. The first measurement we will show on the 5-slot ATCA backplane is the fabric impedance. The characteristic impedance of the transmission line is defined by the ratio of the voltage and current at any point as a test pulse travels down a pair of differential backplane traces. [1]. Impedance mismatches (due to vias and connectors) and variations can cause reflections, which degrade the signal quality.

Time Domain Reflectometry (TDR) produces a positive-going incident wave that is applied to the device under test (DUT). The step-pulse travels down the DUT at the velocity of propagation of the line. If the load impedance is equal to the characteristic impedance of the line, no wave is reflected and all that will be seen on the oscilloscope is the incident voltage step recorded as the wave passes the point on the line monitored by the oscilloscope. At every impedance discontinuity that the signal encounters, part of the incident wave is reflected. The reflected voltage wave will appear on the osci loscope [2]. The resulting waveform is like a road map of the impedance variations across the trace.

The worst case connection paths were tested only. That means the longest net length traces were tested. The differential impedance of the backplane and board serial links for Base and Fabric interfaces should be 100 Ohm+- 10%. The measured average value of differential trace line is 107 ohm. Even the worst-case scenario performed within the required range.

For our measurements, we used a wide-bandwidth oscilloscope with 18 GHz measuring bandwidth, high-quality cables, termination resistors, and IConnect analysis software from TDA systems.

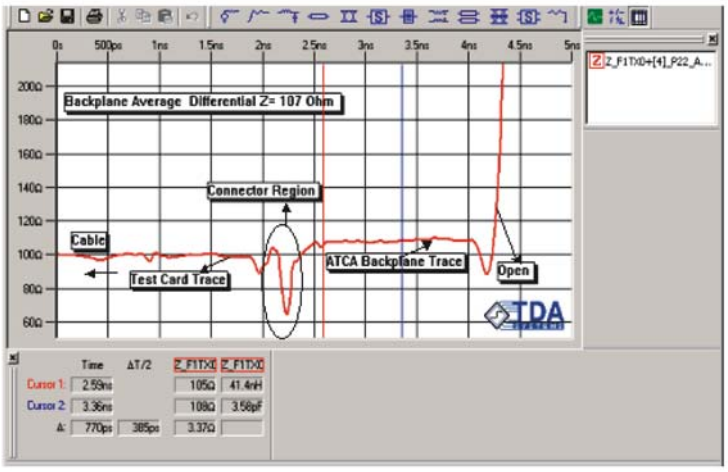
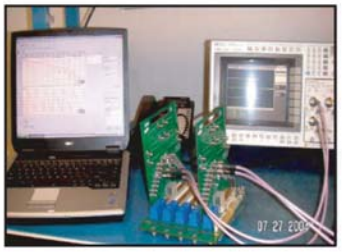


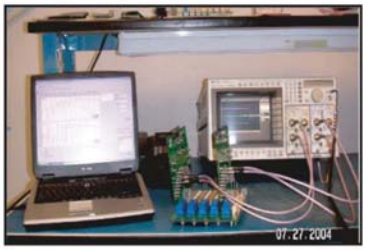
Fig1: Layer09_Slot01_P22_AB7 Impedance Waveform

S-Parameter

Scattering parameters can capture the reflection and transmission from junctions in backplanes. The ratio of the reflected power to the incident power is the return loss and the ratio of the transmitted power to the incident power is the Insertion loss. These values are derived for defined incremental frequency steps over a range of frequencies that covers the design requirements for the backplane. For AdvancedTCA this was the range from 0 to 5 GHz.

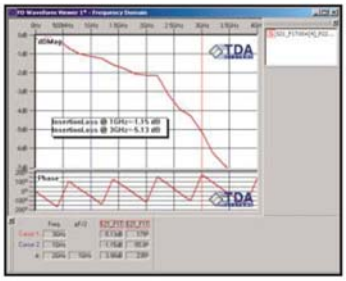


S21 Test Set Up



S11 Test Set Up

The results show that both the Insertion and Return Loss on the 5-slot ATCA backplane under test do not violate the Insertion loss and Return limits for PICMG 3.0.

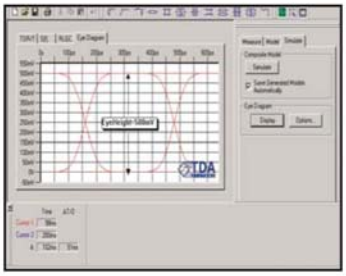


Layer09_Sig04_AB7 _S21 Waveform

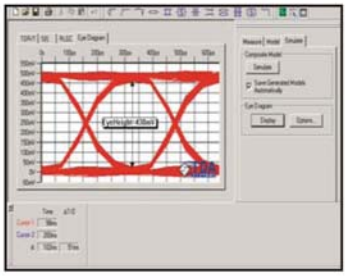
Layer11_Sig05_AB8_S1 Waveform

Eye Diagram

An eye diagram takes the results of a simulation driven by a long, multi-cycle bi sequence, superimposes each bit period over the top of all others—like a time exposure photograph—and presents waveforms that have open areas shaped something like a human eye. The larger the eye opening, the better the results. The most common type of stimulus used in eye-diagram generation is the "PRBS" or "pseudo-random bit sequence." [3] From the result, we can see, trace on layer nine which is routed on slot1 to slot5 still has a more than adequate eye opening (86%) at a PRBS 2^10-1 of 3.125Gbps.



3.125Gbps Reference Eye Height: 500mV



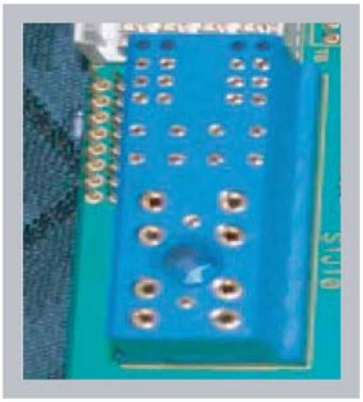
Slot1 to Slot 5 Eye Height: 430mV

Performance Assured

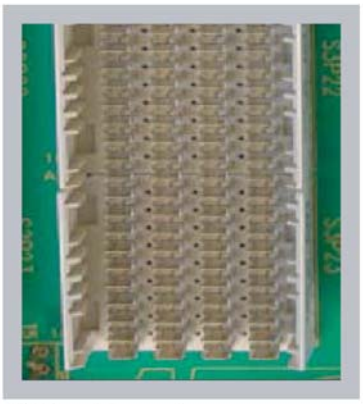
As you can see from the results above, we were able to show that the 5-slot ATCA backplane performance was well within the specified requirements, even taking the worst-case scenarios. Simulation and characterization capabilities will be increasingly important as we continue to move to higher-speed switch fabric technologies.

Elma Bustronic will continue to publish various SI studies in the coming months. This includes a study on pre-design simulation of an AdvancedTCA backplane. If you have any questions or would like further information of SI capabilities and studies, visit www.elmabustronic.com or contact us at 510-490-7388.

Power Studs



VBP Power Connector



ZD Signal Connectors

Design Elements

Power Distribution

The Elma Bustronic ATCA backplane family uses the Positronic VPB series, part number VPB30W8F9300A1. Adequate numbers of 48V 6/32 studs are distributed throughout the backplane.

Materials and Finishes - VPB
Insulator: Glass-filled polyester, UL 94V-0, blue color.
Contacts: Precision-machined copper alloy with gold flash over nickel plate.

Electrical Characteristics -VPB
Contact Current Ratings, per UL 1977
Size 16 Power Contacts: 30 amperes continuous, all contacts under load.
Size 22 Signal Contacts: 2 amperes nominal rating.
Initial Contact Resistance;
Termination to termination:
Size 16 Contacts: 0.0022 ohms maximum,
Size 22 Contacts: 0.0085 ohms maximum,
Per IEC 512-2, Test 2b.
Working Temperature: -55°C to +125°C.

Common Contact Position Function - VPB
1-16 Low Speed Hardware Management
17-24 High Voltage Metallic Test and Ringing Generator Signals
25 Shelf Ground
26 Logic Ground
27/32 Enables for A and B power
28 A Return
29 B Return
30 A Early
31 B Early
33 A Voltage
34 B Voltage

Signal Connectors

The ZD connector is designed to handle over 5 Gbps speeds over standard FR-4 PCB material. The design includes shielded differential pair signal pins for high-performance.

Other Connectors

Shelf Management Connectors

Shmc1 connector goes to the Shmc port on slot 1.
Shmc2 connector goes to the Shmc port on slot 2.

Metal and Ring Connectors

MT1 and MT2 are TYCO 880222-4. It mates to an EI Series receptacle with crimp termination, such as 172142-4 There is also an MT EI Series with IDC termination.

Ring Connector

The Ring connector is a Molex 71231-0005 which mates with the Molex 71694 and 5557 series.

GLOSSARY

DUAL STAR TOPOLOGY

A fabric topology in which two switch resources provide redundant connections to all end points within the network. The Base Interface is defined as a Dual Star fabric topology for all PICMG 3.0 compliant backplanes. For the Fabric Interface, Dual Star provides the minimum redundant fabric environ ment required for compliant backplane configuration. Up to 14 Node Board/Slots utilize two Fabric Channels to support a connection to each of two Fabric Boards/Slots. Fabric Boards/Slots support a connection to all Node Boards/Slots within a shelf and to the other FabricBoard/Slot.

DUAL-DUAL STAR TOPOLOGY

A fabric topology in which four switch resources provide redundant connections to all end points within the network. Dual-Dual Star configurations may be supported within the Fabric Interface to provide a single highly redundant fabric environment or two redundant fabrics between all boards/slots within a shelf. Up to 12 Node Board/ Slots utilize four Fabric Channels to support a connection to each of 4 Fabric Boards/Slots. Fabric Boards/Slots support a connection to all Node Boards/Slots within a shelf and to the other Fabric Boards/Slots.

FULL MESH TOPOLOGY

A fabric topology in which all network end-points have a direct connection to all other end-points. Full Mesh configurations maybe supported within the Fabric Interface to provide a highly redundant fabric environment capable of very large aggregate bandwidth capacity across the shelf. Full Mesh configured backplanes are capable of supporting Mesh Enabled Boards or Fabric and Node Boards installed in a dual star arrangement.

REPLICATED MESH TOPOLOGY

Because mesh configurations have a distributed fabric they are best suited for these smaller systems since all slots can support processing boards and none need be dedicated to support switching resources. Another approach possible in reduced slot backplanes is to replicate the mesh between slots/boards. Thus signal capacities between boards may be increased between boards in a reduced slot backplane.

BASE INTERFACE

A Zone 2 interface that is used to support 10/100 or 1000BASE-T connections between Boards in a shelf. Backplanes are required to support the Base Interface by routing 4 differential signal pairs between all Node Slots and each Fabric Slot (Logical Slots 1 & 2) Boards may support the Base Interface. If the Fabric interface does not support IP, it is expected that the Base Interface will be used for carrying IP management data between boards within a shelf.

BASE CHANNEL

A physical connection within the Base Interface composed of up to 4 differential signal pairs (1 row) along the Zone 2 ZD connector. Base Channels are mapped to ZD connectors J23/P23 and J24/P24. Base Channels are numbered 1 through 16. Each Base Channel is the endpoint of a slot-to-slot connection within the Base Interface. A Node Slot/Board supports Base Channels 1 & 2 and establishes connections to Logical Slots 1 & 2 respectively. A Base Fabric Slot/Board resides in Logical Slots 1 & 2 and supports connections to al Node/Slots/Boards.

FABRIC ITERFACE

A Zone 2 interface that provides connections comprised of up to 8 differential signal pairs (Channel) between end-points. Compliant backplanes may support the Fabric Interface in a variety of configurations including Full Mesh and Dual Star topologies. Boards that support the Fabric Interface may be configured as Node Boards, Fabric Boards or Mesh Enabled Boards. Compliant board implementations of the Fabric Interface are defined by the PICMG 3.x subsidiary specifications.

FABRIC CHANNEL

A physical connection within the Fabric Interface composed of up to 8 differential signal pairs (2 adjacent rows) along the Zone 2 ZD connector. Fabric Channels are mapped to ZD connectors J20/P20 through J23/P23. Any system slot in a backplane may support between 2 to 15 Channels. Each Fabric Channel is the endpoint of a slot-to-slot connection such that a system slot/board with 2 Channels supports connections to 2 other systems slots/boards. Fabric Channels are numbered 1 through 15 and slots/boards always support them in sequential order starting with Fabric Channel 1. Fabric Channels are sub-divided into four 2-pair Ports and may be Single Port (2-pair), Double Port (4-pair) or Full Channel (8-pair) implementations.